

REMARKS/ARGUMENTS

Further to the amendment filed January 24, 2003, applicant has clarified the language of claims 17, 24, 27 and 28.

In addition, new claims 47 – 58 have been added. Claims 47 – 54 are directed to a mirror image stacked memory cell arrangement having a common electrode which is not taught or suggested by the cited references. This subject matter is illustrated, for example, in Figure 6. New claims 55 – 57 have also been added and are copied claims 32, 33 and 58 from published application 2002/0168820 A1, a copy of which was furnished in an IDS filed on December 18, 2003 in the instant application.

A proposed drawing correction for Figure 1 is also attached. Although field isolation areas 100 are clearly identified in Figure 1, applicant proposes to modify Figure 1 to show the isolation regions using a more conventional and well know format.

Consideration of this Supplemental Amendment, together with the Amendment of January 24, 2003, is respectfully requested.

Dated: January 27, 2003

Respectfully submitted,

By 

Thomas J. D'Amico

Registration No.: 28,371

DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP

2101 L Street NW

Washington, DC 20037-1526

(202) 785-9700

Attorneys for Applicant



Version With Markings to Show Changes Made

IN THE CLAIMS:

Please amend the claims as follows.

17. (Twice Amended) A method of fabricating a memory device comprising:

forming a first memory cell to include a chalcogenide glass material having a changeable resistance and cathode and anode electrodes spaced apart and in contact with said chalcogenide glass material;

forming a second memory cell to include a chalcogenide glass material having a changeable resistance and cathode and anode electrodes spaced apart and in contact with said chalcogenide glass material;

forming said anode electrodes of said memory cells as a common anode [for both of said first and second memory cells], wherein said common anode comprises a middle conductive layer and a layer of silver on opposite sides of said middle conductive layer.

24. (Twice Amended) A method as in claim 23 further comprising forming a column line conductor electrically coupled to a second active region of a first access transistor.

27. (Twice Amended) A method as in claim 26 wherein said first and second memory cells are formed to be coupled to different column lines by said first and second access transistors.

28. (Twice Amended) A method as in claim 17 wherein said first and second memory cells are formed to be connected to the same column line by said first and second access transistors.